

Computer and Network Security

Lecture 15: Hardware Security

COMP-5370/6370
Fall 2024



Trusted Computing Base



The **Trusted Computing Base (TCB)** is the collection of all components within a system critical to providing security properties.

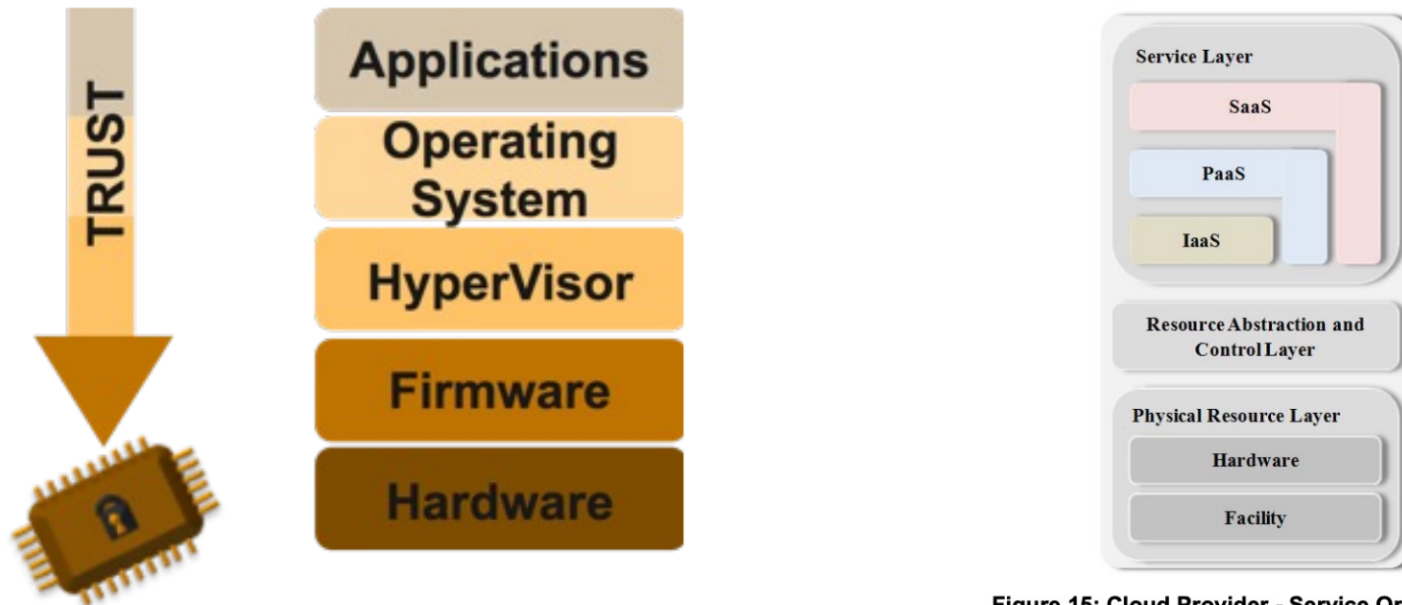
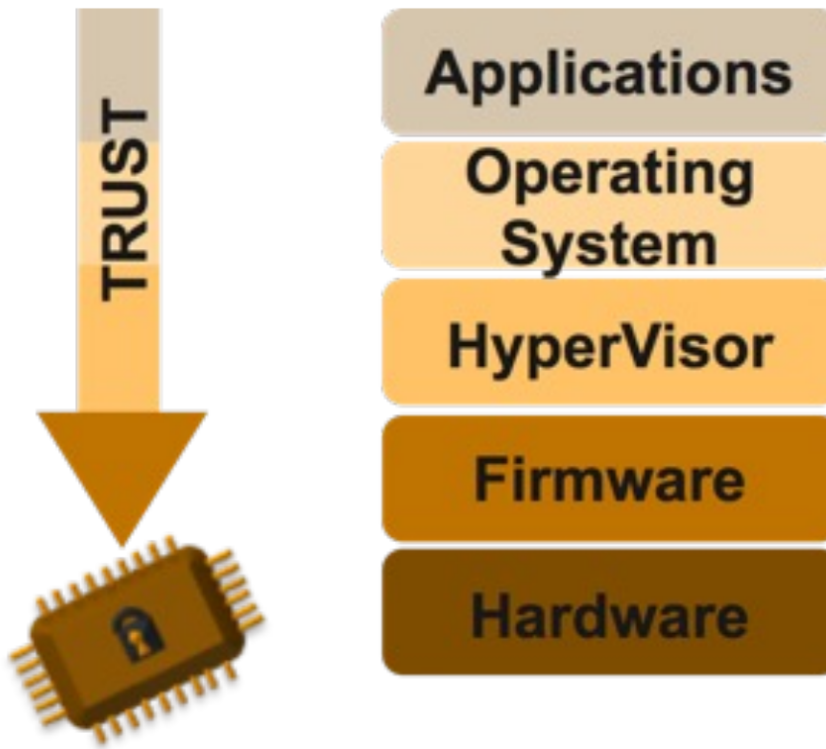


Figure 15: Cloud Provider - Service Orchestration

Local TCB



- Everything needed to run the application safely
- Each layer relies on the layers below it to behave correctly

Let's Connect to a Server



Let's Connect to a Server



- Bash Environment

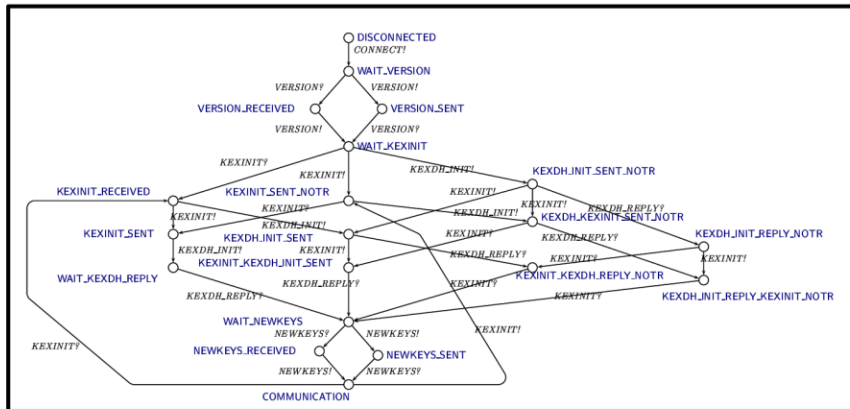
```
$>  
$> ssh username@host
```

```
$> which ssh  
/tmp/malwarehooks/ssh
```

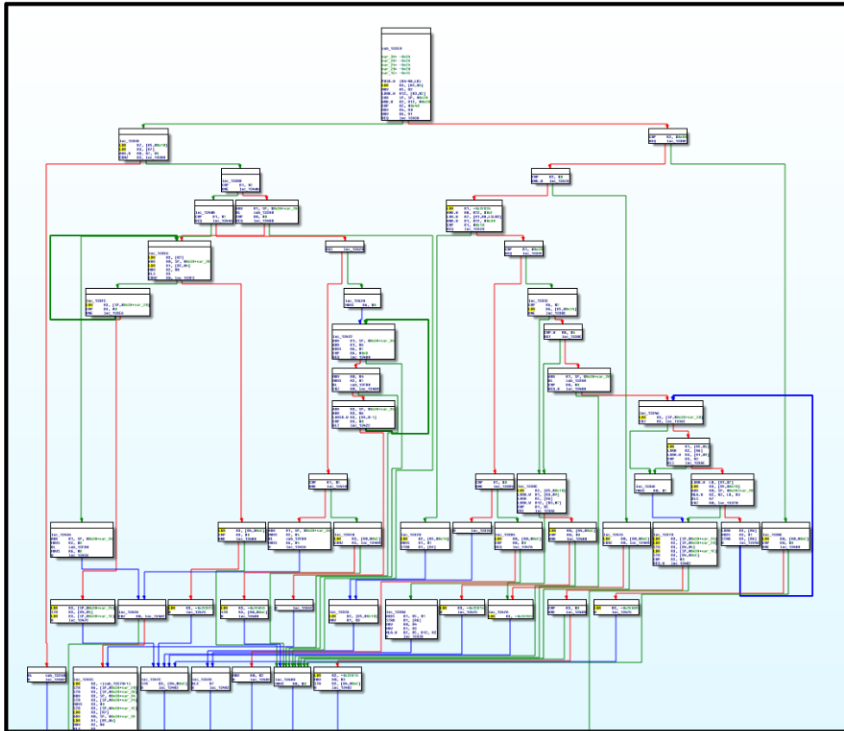
Let's Connect to a Server



- Bash Environment
- SSH protocol design



Let's Connect to a Server



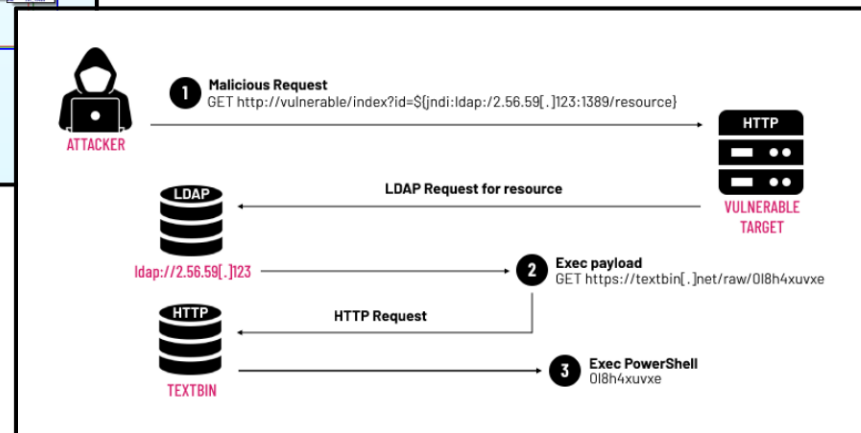
- Bash Environment
- SSH protocol design
- SSH app architecture

Let's Connect to a Server

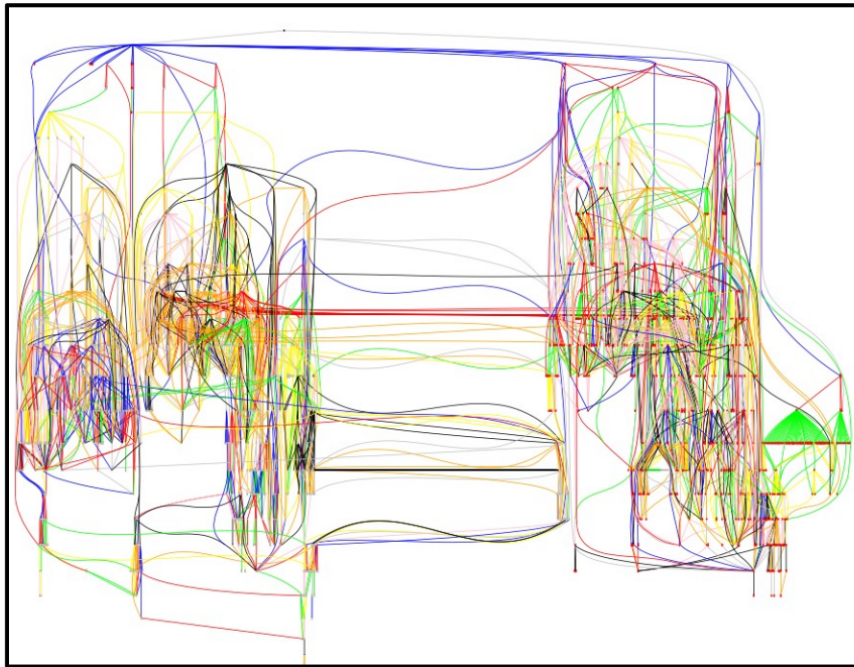


The screenshot shows an Ars Technica article titled "Zero-day in ubiquitous Log4j tool poses a grave threat to the Internet". The article is by Dan Goodin, dated December 9, 2021. The sub-headline reads "Minecraft is the first, but certainly not the last, app known to be affected." The article content is partially obscured by a red and white binary code graphic. The Ars Technica logo and navigation links are visible at the top of the page.

- Bash Environment
- SSH protocol design
- SSH app architecture



Let's Connect to a Server



- Bash Environment
- SSH protocol design
- SSH app architecture
- SSH app logic

Let's Connect to a Server



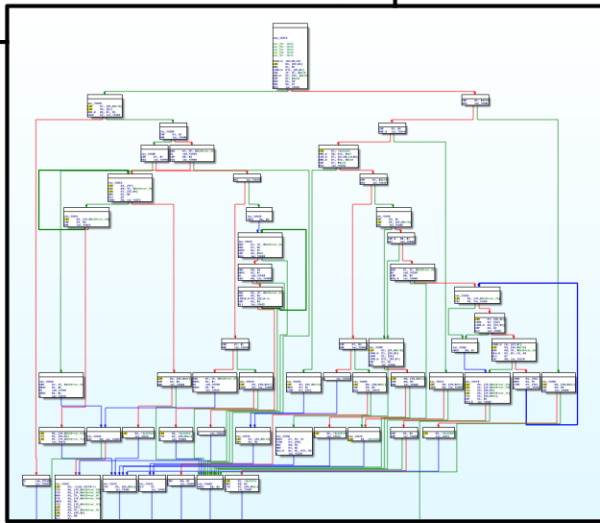
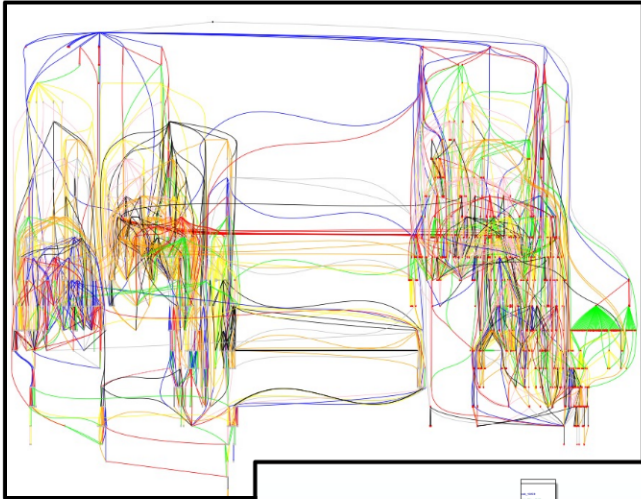
$SEC_k : \text{Hon}(\hat{C}, \hat{K}) \supset (\text{GoodKeyAgainst}(X, k) \vee \hat{X} \in \{\hat{C}, \hat{K}\})$	
$SEC_{akey} : \text{Hon}(\hat{C}, \hat{K}, \hat{T}) \supset (\text{GoodKeyAgainst}(X, AKey) \vee \hat{X} \in \{\hat{C}, \hat{K}, \hat{T}\})$	
$SEC_{skkey} : \text{Hon}(\hat{C}, \hat{K}, \hat{T}, \hat{S}) \supset (\text{GoodKeyAgainst}(X, SKey) \vee \hat{X} \in \{\hat{C}, \hat{K}, \hat{T}, \hat{S}\})$	
$AUTH_{kas} : \exists \eta. \text{Send}((\hat{K}, \eta), \text{Cert}_K.SIG[sk_K](\text{"DHKey"} .gy.\tilde{n}_1).E_{sym}[k_{T,K}^{\hat{t} \rightarrow k}](AKey.\hat{C}).E_{sym}[k](AKey.n_1.\hat{T}))$	
$AUTH_{tgs} : \exists \eta. \text{Send}((\hat{T}, \eta), \hat{C}.E_{sym}[k_{S,T}^{\hat{s} \rightarrow \hat{t}}](SKey.\hat{C}).E_{sym}[AKey](SKey.n_2.\hat{S}))$	
$SEC_k^{client} : [\text{Client}]_C SEC_k$	$SEC_k^{kas} : [\text{KAS}]_K SEC_k$
$SEC_{akey}^{client} : [\text{Client}]_C SEC_{akey}$	$AUTH_{kas}^{client} : [\text{Client}]_C \text{Hon}(\hat{C}, \hat{K}) \supset AUTH_{kas}$
$SEC_{akey}^{kas} : [\text{KAS}]_K SEC_{akey}$	$AUTH_{kas}^{tgs} : [\text{TGS}]_T \text{Hon}(\hat{T}, \hat{K})$
$SEC_{akey}^{tgs} : [\text{TGS}]_T SEC_{akey}$	$\supset \exists n_1, k, gy, \tilde{n}_1. AUTH_{kas}$
$SEC_{skkey}^{client} : [\text{Client}]_C SEC_{skkey}$	$AUTH_{tgs}^{client} : [\text{Client}]_C \text{Hon}(\hat{C}, \hat{K}, \hat{T}) \supset AUTH_{tgs}$
$SEC_{skkey}^{tgs} : [\text{TGS}]_T SEC_{skkey}$	$AUTH_{tgs}^{server} : [\text{Server}]_S \text{Hon}(\hat{S}, \hat{T})$
	$\supset \exists n_2, AKey. AUTH_{tgs}$

Table 1. DHINIT Security Properties

$$\begin{aligned}
 C &\longrightarrow K(I) : \text{Cert}_C.SIG[sk_C](\text{"Auth"}.HASH(\hat{C}.\hat{T}.n_1.\tilde{n}_1.gx).\hat{C}.\hat{T}.n_1) \\
 I &\longrightarrow K : \text{Cert}_I.SIG[sk_I](\text{"Auth"}.HASH(\hat{I}.\hat{T}.n_1.\tilde{n}_1.gx).\hat{I}.\hat{T}.n_1) \\
 K &\longrightarrow I \longrightarrow C : \text{Cert}_K.SIG[sk_K](\text{"DHKey"} .gy.\tilde{n}_1). \\
 &\quad E_{sym}[k_{T,K}^{\hat{t} \rightarrow k}](AKey.\hat{I}).E_{sym}[k](AKey.n_1.\hat{T})
 \end{aligned}$$

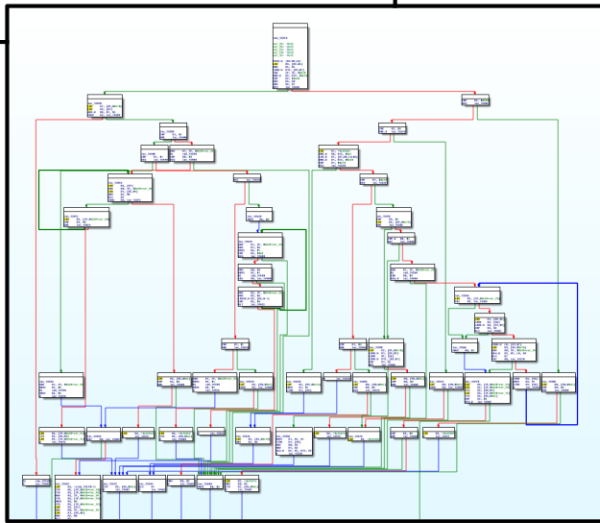
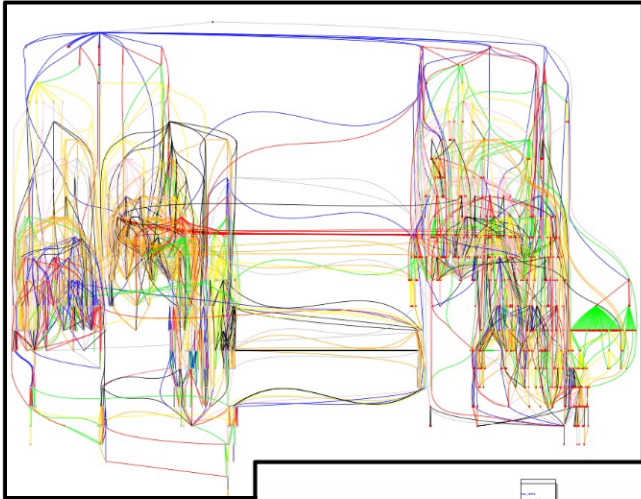
- Bash Environment
- SSH protocol design
- SSH app architecture
- SSH app logic
- Crypto math

Let's Connect to a Server



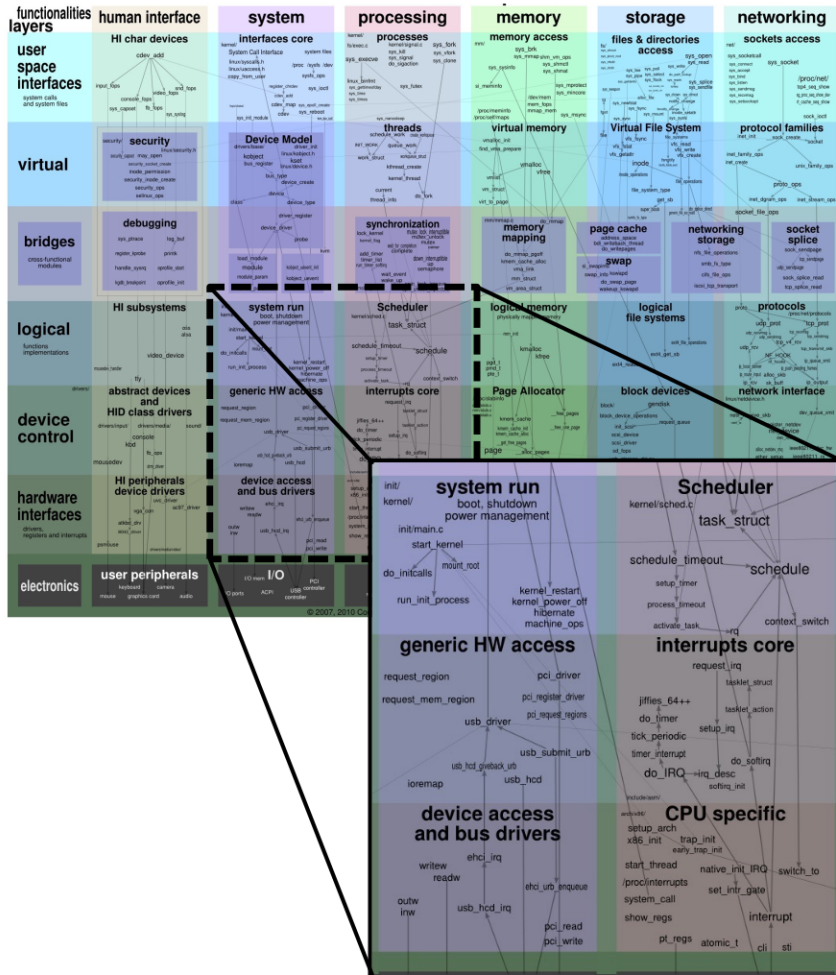
- Bash Environment
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- Crypto math
- Crypto implementation

Let's Connect to a Server



- Bash Environment
- SSH protocol design
- SSH app architecture
- SSH app logic
- Crypto math
- Crypto implementation
- Channel design
- Channel implementation

Let's Connect to a Server



- Bash Environment
- SSH protocol design
- SSH app architecture
- SSH app logic
- Crypto math
- Crypto implementation
- Channel design
- Channel implementation
- OS implementation

Android is Notorious



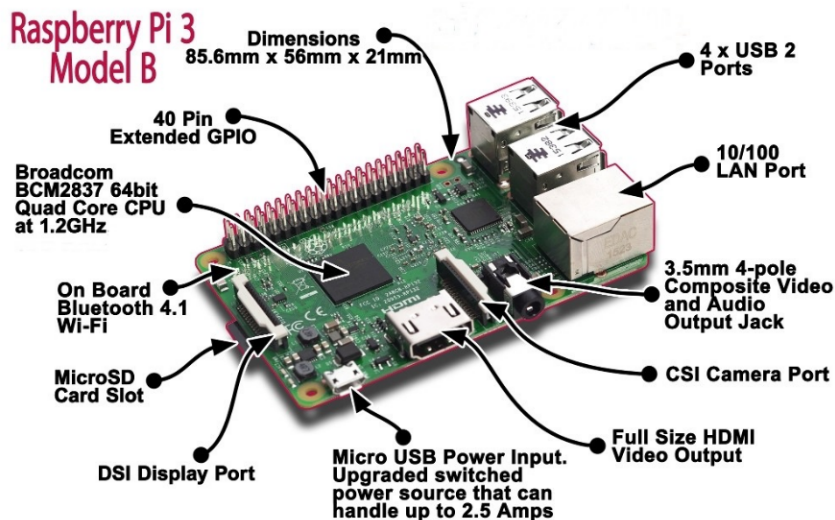
A screenshot of an Ars Technica article. The header shows the 'ars TECHNICA' logo, a 'SUBSCRIBE' button, and a 'SIGN IN' dropdown menu. The article title is 'Powerful backdoor/rootkit found preinstalled on 3 million Android phones'. Below the title is a sub-headline: 'Firmware that actively tries to hide itself allows attackers to install apps as root.' The author is 'DAN GOODIN' and the date is '11/18/2016, 12:12 PM'.

A screenshot of a ZDNet article. The header includes the 'ZDNet' logo, a search icon, a 'MENU' button, a user profile icon, and 'US'. A 'MUST READ' section is visible with the title 'Agile development: How to tackle complexity and get stuff done'. The main article title is 'Android Trojan infiltrates mobile firmware, Trend Micro apps'. A sub-headline reads: '[UPDATED] The ad-serving malware has been spotted in the firmware of roughly 40 smartphones and a number of popular mobile apps.' Below the title are social media sharing icons for LinkedIn, Facebook, Twitter, Email, and Print. The author is 'By Charlie Osborne for Zero Day | March 18, 2016 -- 13:05 GMT (06:05 PDT) | Topic: Security'.

A screenshot of a Wired article. The header shows the 'WIRED' logo, navigation links for 'BACKCHANNEL', 'BUSINESS', 'CULTURE', 'GEAR', and 'MORE', and a 'SIGN IN' button. The author is 'DAVID KRAVETS' and the date is '12.16.2011 08:00 PM'. The article title is 'Mobile Carriers Claim Consumer Consent to Carrier IQ Spying'. The sub-headline reads: 'Two of the nation's largest wireless phone providers say their customers authorized them to secretly monitor their phone, thanks to the small print in the contracts millions have signed and few have read.' Below the title are social media sharing icons for Facebook, Twitter, Email, and Print.

- “System” apps are 3P apps that are treated as part of the OS
- Pre-installed apps that can't be uninstalled
 - Carrier IQ was first major one (2011)
 - Far from the only

Let's Connect to a Server



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- Channel implementation
- OS implementation
- Firmware for HW

Lenovo Firmware Rootkit



A screenshot of the website 'The Hacker News'. The main article title is 'Lenovo Caught Using Rootkit to Secretly Install Unremovable Software'. Below the title is a screenshot of a Windows 8.1 desktop environment. Red arrows point from the article text to specific elements on the desktop: the 'Xbox Console' tile, the 'Office' tile, the 'OneNote' tile, the 'FRIENDS' tile, the 'Microsoft Solitaire Collection' tile, and the 'Photos' tile. The desktop also shows a 'Tuesday 4' tile, a 'Mail' tile, and an 'Explore' section with a 'Store' and 'e' tile.

Lenovo Service Engine (LSE) BIOS for Notebook

Lenovo Security Advisory: LEN-2015-020

Potential Impact: Privilege Escalation

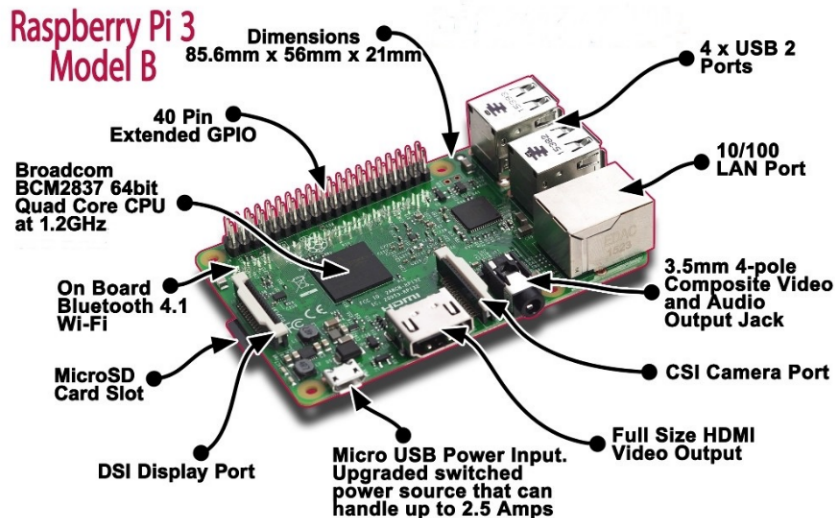
Severity: High

Summary:

Vulnerabilities have been identified in the Lenovo Service Engine (LSE) which may run on certain Lenovo notebook systems that do not have a Lenovo preloaded operating system installed. Lenovo has released a BIOS update to disable Lenovo Service Engine and a utility to remove services and files left on the system for systems running Windows 7, 8, 8.1 and 10. See below for a full list of notebook systems with LSE installed. This issue has been assigned CVE-2015-5684.

- BIOS replaces Win7-10 OS files during boot
- Sent device-specific info to corp. on 1st boot
- Automatically installed applications in OS
 - Auto-updates for drivers
 - Bloat-ware
- Had exploitable vulnerabilities

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- Firmware for HW
- HW components

Rowhammer



Project Zero

News and updates from the Project Zero team at Google

Monday, March 9, 2015

Exploiting the DRAM rowhammer bug to gain kernel privileges

Posted by Mark Seaborn, sandbox builder and breaker, with contributions by Thomas Dullien, reverse engineer

[This guest post continues Project Zero's practice of promoting excellence in security research on the Project Zero blog]

- Allows arbitrary process to flip bits in physical memory
- Predictable but not 100% perfect

Think of all the things you can do with 1 bit.

ars TECHNICA

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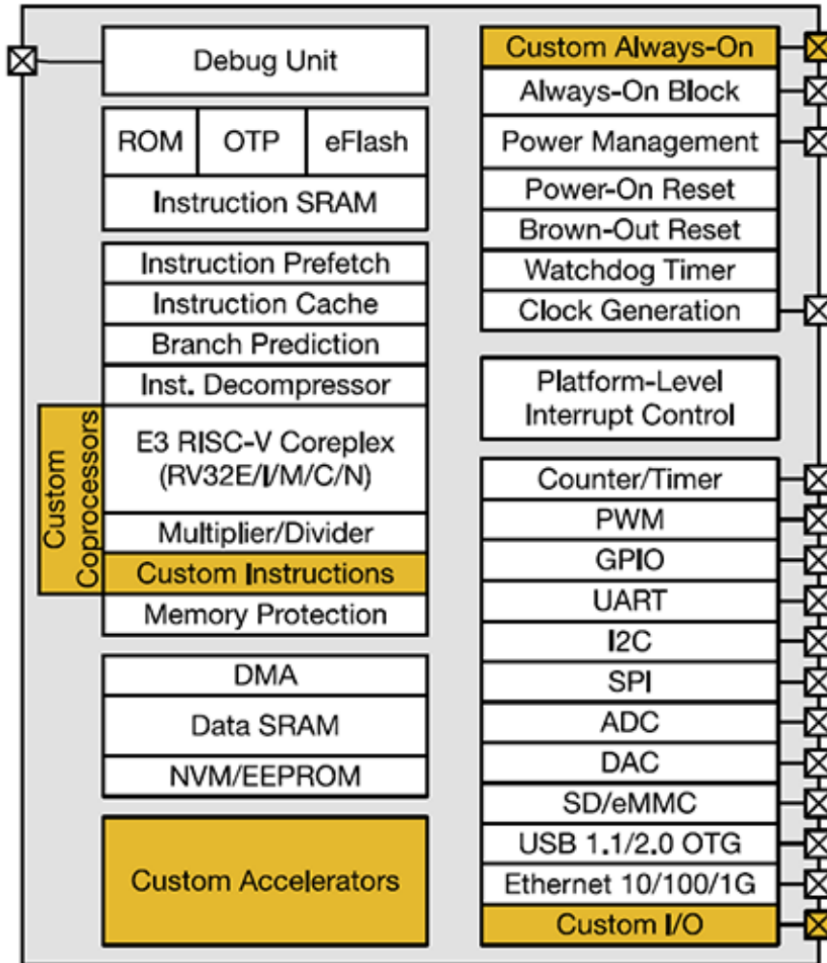
RAMBLEED —

Researchers use Rowhammer bit flips to steal 2048-bit crypto key

RAMbleed side-channel attack works even when DRAM is protected by error-correcting code.

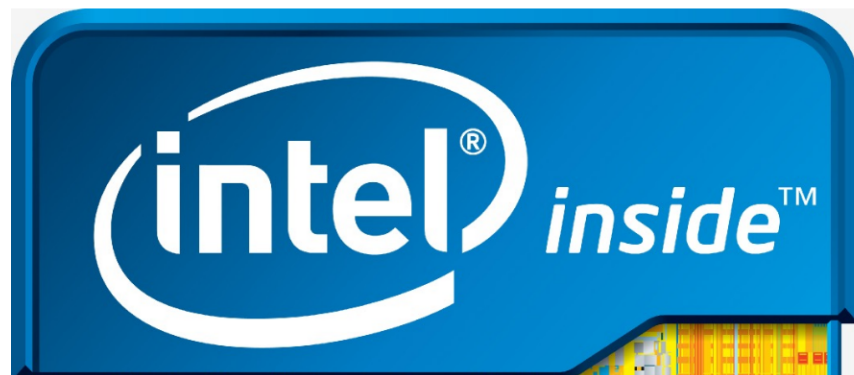
DAN GOODIN - 6/11/2019, 12:00 PM

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- OS implementation
- Firmware for HW
- HW components
- SoC design/impl.
- Chip design/impl.

CPU Management



The Intel Management Engine is Really Rather Scary

This closed source non-auditable subsystem [can](#):

- Access all areas of your computer's memory, without the CPU's knowledge.
- Access every peripheral attached to your computer.
- Set up a TCP/IP server on your network interface that can send and receive

WIRED BACKCHANNEL BUSINESS CULTURE GEAR MORE SIGN IN

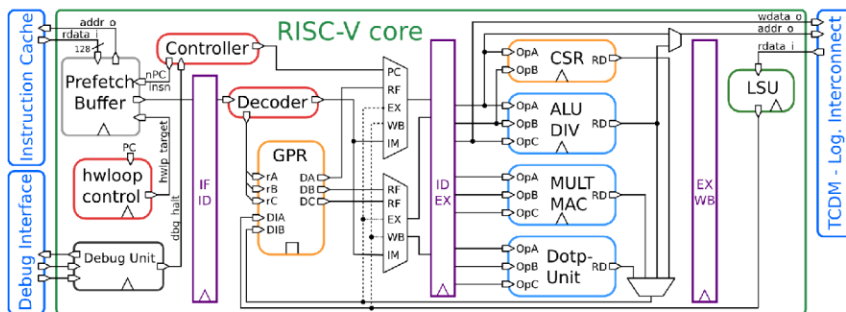
LILY HAY NEWMAN SECURITY 11.20.2017 11:10 PM

Intel Chip Flaws Leave Millions of Devices Exposed

Security experts have warned of Intel's Management Engine for years. A new set of confirmed vulnerabilities that impact PCs, servers, and IoT devices shows they may have been right.

- Completely separate co-processor built into Intel CPUs
- AMD Platform Security Processor (AMD PSP)
 - All chips since 2013
- Intel Management Engine (Intel ME)
 - All chips since 2008


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- Firmware for HW
- SoC design/impl.
- CPU design/arch

CPU Bugs





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CPU Bugs

Computers are made by humans, and thus inherently prone to errors. This page describes known bugs for various models and brands.

Contents [\[hide\]](#)

- 1 Affecting almost all modern architectures
 - 1.1 Spectre
- 2 x86 misfeatures
 - 2.1 ESP is not cleared
 - 2.1.1 Mitigations
 - 2.2 NULL selector load may not clear MSR_GS_BASE
 - 2.2.1 Mitigations
 - 2.3 FXSAVE/FNSAVE
 - 2.4 SYSRET
 - 2.4.1 Mitigations
 - 2.5 SS selector
 - 2.5.1 Mitigation
 - 2.6 PUSH selector
 - 2.6.1 Mitigation
 - 2.7 Nesting of NMI interrupt
- 3 Intel
 - 3.1 Transactional Synchronization eXtensions (TSX) Bug
 - 3.2 Extended Page Table (EPT) Bug
 - 3.3 F00F Bug
 - 3.4 FDIV bug
 - 3.5 Buggy HLT
 - 3.6 Core-microarchitecture Bugs
 - 3.7 'Meltdown' Page Table Bug
- 4 AMD
 - 4.1 DragonFly BSD Heavy Load Crash
 - 4.2 Ryzen Bug
 - 4.3 CPUID Bugs
- 5 Cyrix
 - 5.1 Coma Bug

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CPU Bug Examples



Pentium FDIV Bug

```
c = 4195835 / 3145727
```

appeared to be an instance of the worst-case error. Coe did his analysis without actually using a Pentium—he doesn't own one. To verify his prediction, he had to bundle his year-and-a-half-old daughter into his car, drive to a local computer store, and borrow a demonstration machine.

The true value of Coe's ratio is

```
c = 1.33382044 . . . .
```

But computed on a Pentium, it is

```
c = 1.33373906 . . . .
```

Cyrix Coma Bug

```
unsigned char c[4] = {0x36, 0x78, 0x38, 0x36};
int main()
{
    asm (
        "        movl    $c, %ebx\n"
        "again:  xchgl   (%ebx), %eax\n"
        "        movl    %eax, %edx\n"
        "        jmp     again\n"
    );
}
```

HALT AND CATCH FIRE (HCF):

An early computer command that sent the machine into a race condition, forcing all instructions to compete for superiority at once.

Control of the computer could not be regained.

CPU Microcode



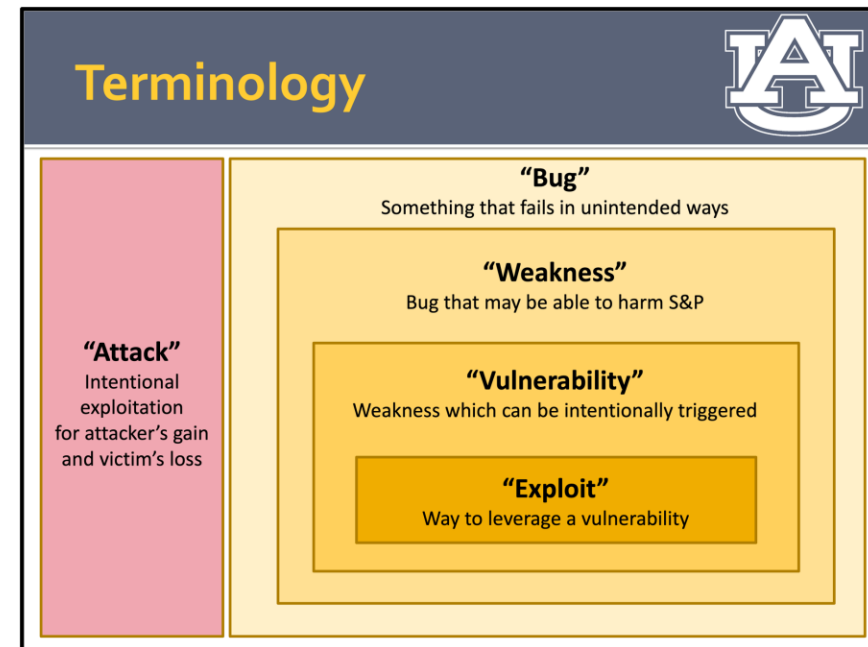
Microcode is firmware that acts as a translator for CPUs and turns *opcodes* into *micro-operations* which are executed.

- RISC won the *RISC vs. CISC War*
 - RISC-style is much more efficient
- Allows manufacturers to patch w/o recall
 - Just install a microcode patch
- **Completely unknown to almost everyone**

Software Facts of Life



- Software has bugs
- Some bugs are weaknesses
- Some weaknesses are vulnerabilities
- Some vulnerabilities can be exploited
- Someone has an interest in exploiting others for gain
- Malware is a different breed of software



Microcode Vulnerabilities



Side Channel Vulnerabilities:
Microarchitectural Data Sampling and
Transactional Asynchronous Abort



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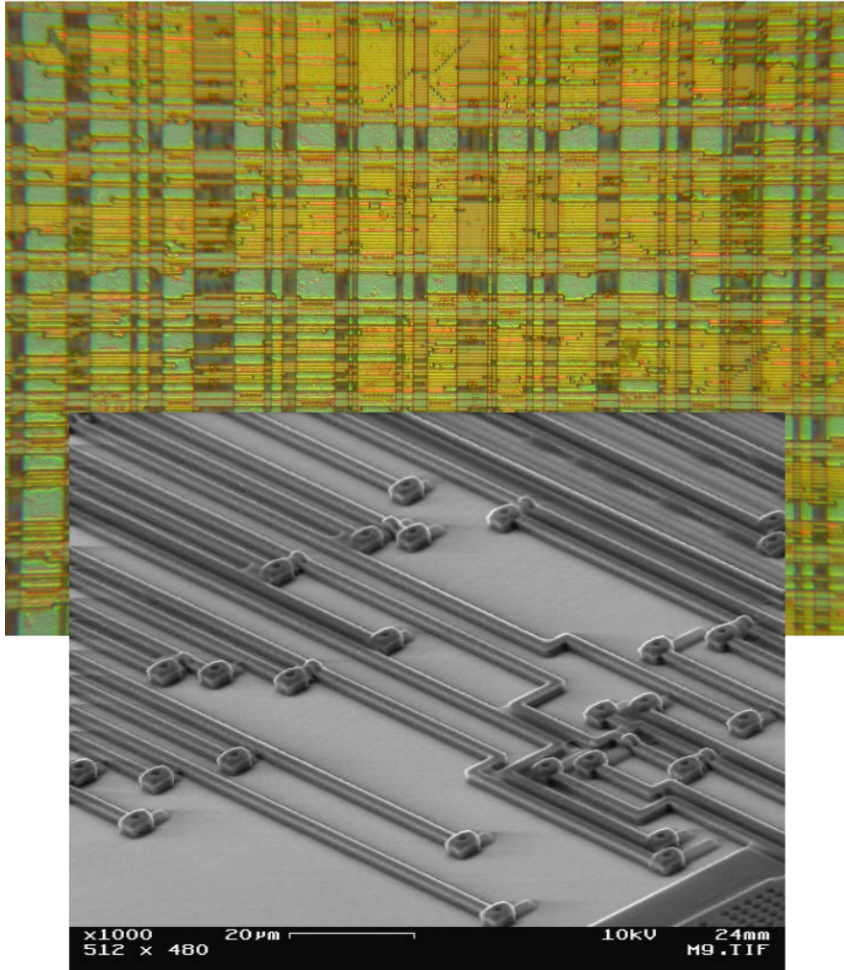
SPECULATIVE EXECUTION STRIKES AGAIN —

Intel SGX is vulnerable to an unfixable flaw that can steal crypto keys and more

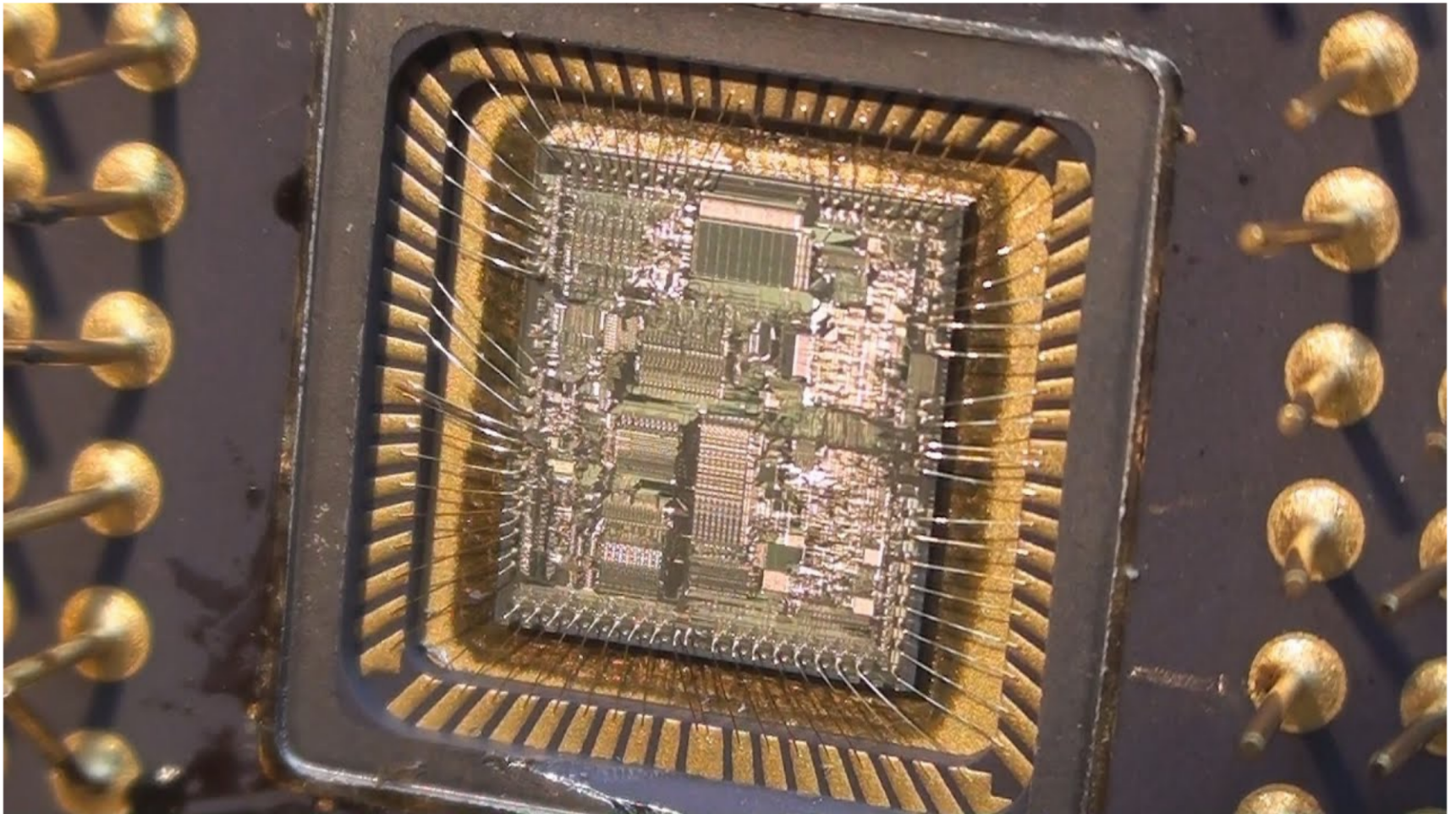
Just when you thought it was secure again, Intel's digital vault falls to a new attack.

DAN GOODIN - 3/10/2020, 5:40 PM

Let's Connect to a Server



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- Channel design
- Channel implementation
- OS implementation
- HW components
- SoC design/impl.
- CPU design/arch
- Sub-component impl.

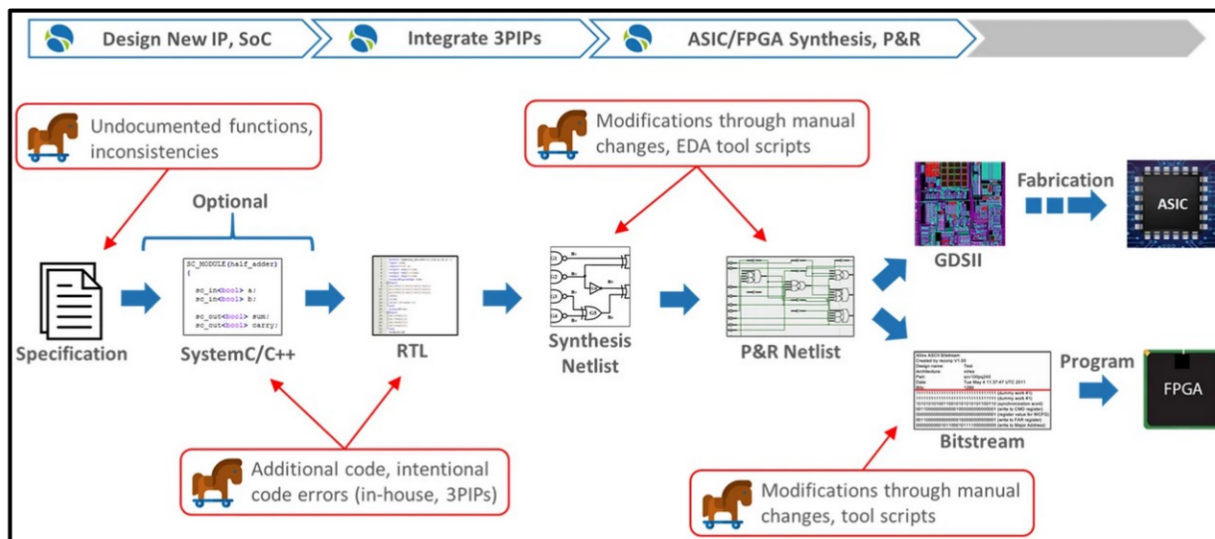


Hardware Trojans



Hardware trojans are just like trojan horse malware except implemented in hardware from the manufacturer.


- Known capability but never seen (AFAIK)




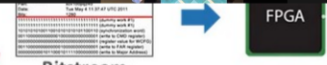
Hardware Trojans



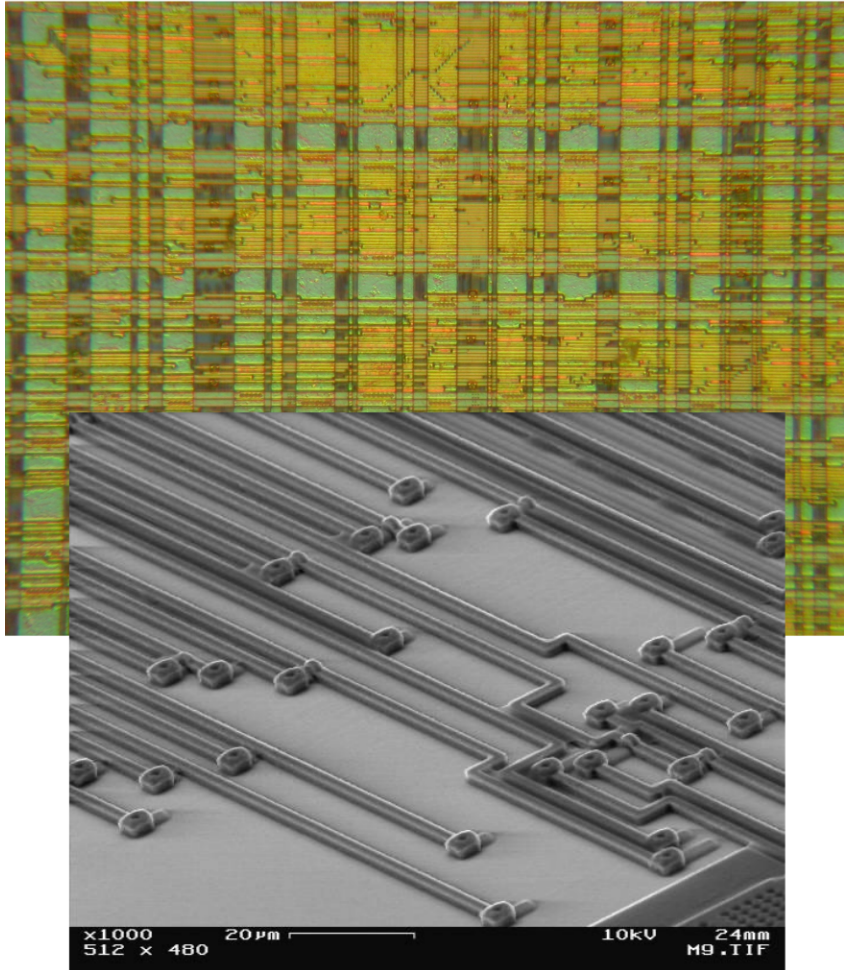
A video player interface showing a presentation slide titled "TSV+Wirebond Cross Section" and a presenter on stage. The slide includes a 3D cutaway diagram of a Target Silicon Chip connected to a Package Substrate via TSV's and Wirebonds. A MITM Implant Chip is shown inserted between the silicon chip and the package substrate. The video player shows a progress bar at 24:19 / 45:37, a title "BlueHat IL 2019 - Andrew 'bunnie' Huang - Supply Chain Security: 'If I were a Nation State...'", and a view count of 16,705 views from Feb 14, 2019.

 Additional code, intentional code errors (in-house, 3PIPs)

 Modifications through manual changes, tool scripts



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- CPU design/arch
- Sub-component impl.
- Silicon traces

Stealthy Dopant Trojans

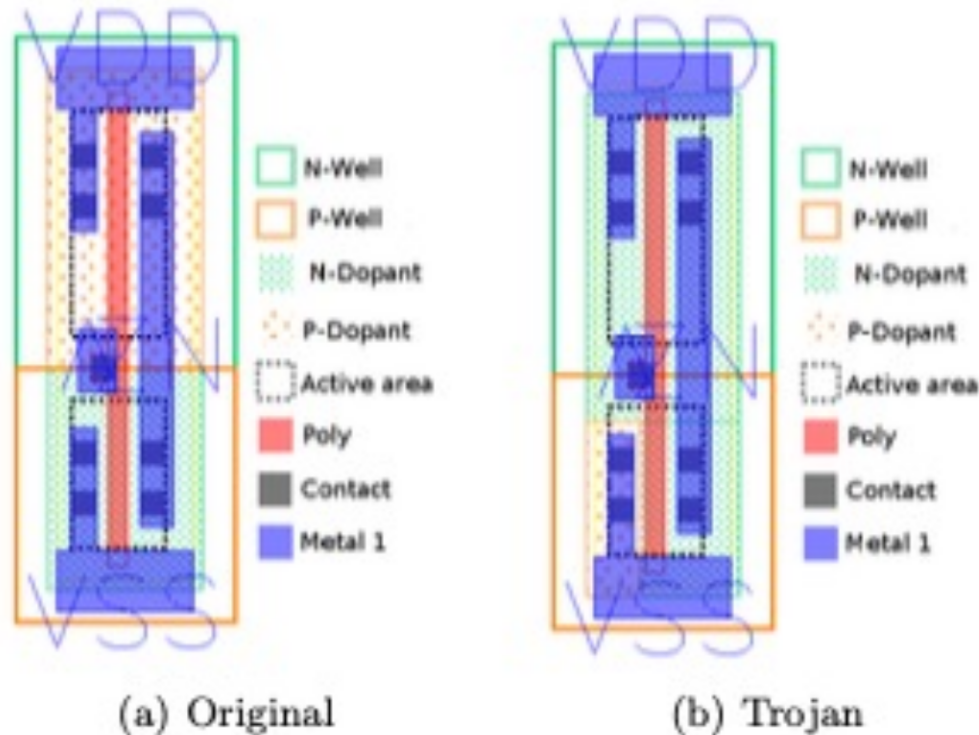


Fig. 1. Figure of an unmodified inverter gate (a) and of a Trojan inverter gate with a constant output of V_{DD} (b).

Stealthy Dopant Trojans

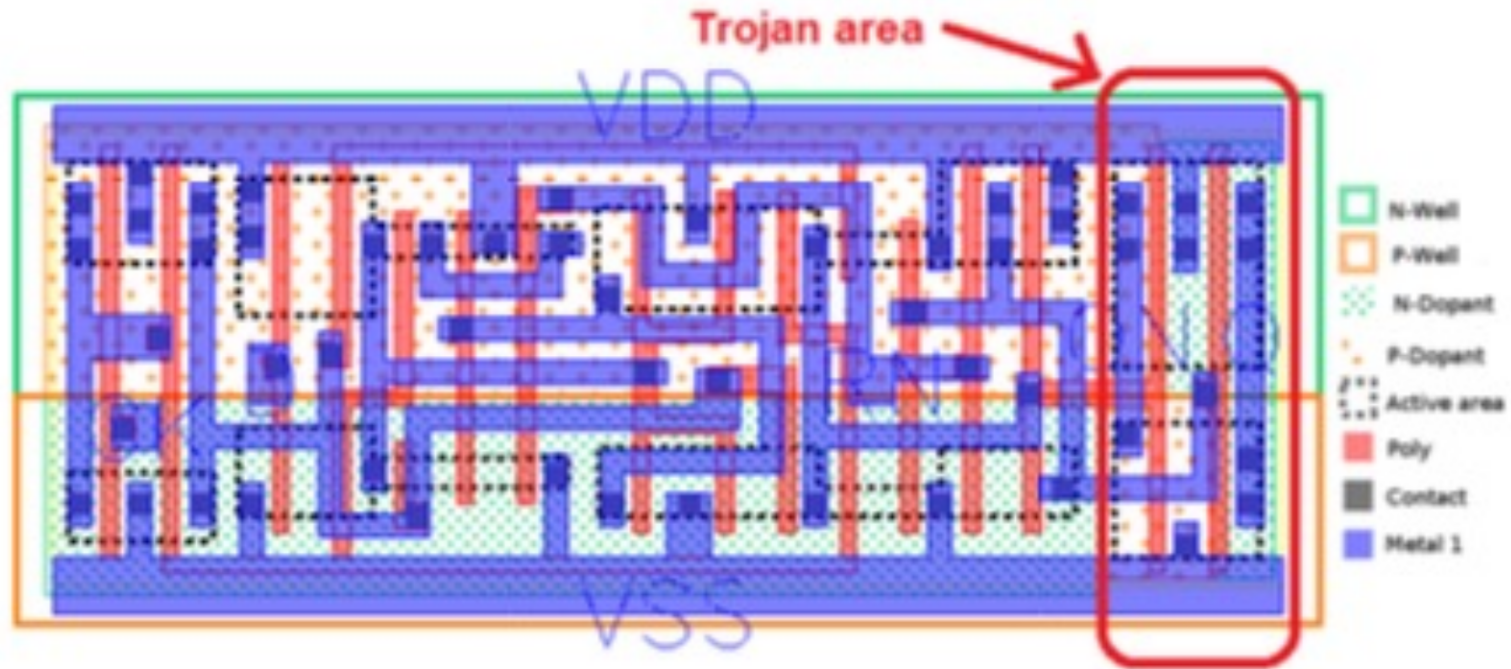


Fig. 2. Layout of the Trojan DFFR_X1 gate. The gate is only modified in the highlighted area by changing the dopant mask. The resulting Trojan gate has an output of $Q = V_{DD}$ and $QN = GND$.

Let's Connect to a Server



boy, that escalated quickly

Trusted Computing Base



The **Trusted Computing Base (TCB)** is the collection of all components within a system critical to providing security properties.

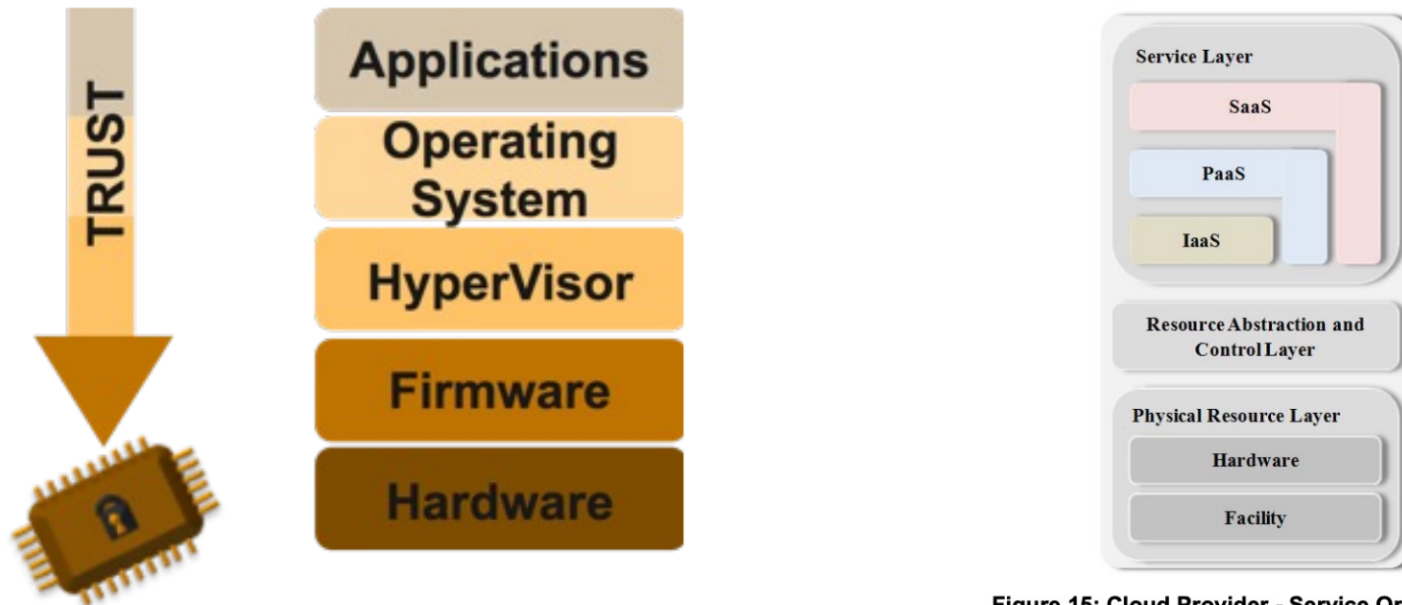


Figure 15: Cloud Provider - Service Orchestration

CPU Instructions



- Low-level commands passed to CPU
- Carried out via physical gates
 - AND, OR, NOT, etc
 - Latches, Counters, Adders, etc

```
section      .text
global      _start                ;must be declared for linker (ld)

_start:     ;tell linker entry point

    mov     edx,len                ;message length
    mov     ecx,msg                ;message to write
    mov     ebx,1                  ;file descriptor (stdout)
    mov     eax,4                  ;system call number (sys_write)
    int     0x80                  ;call kernel

    mov     eax,1                  ;system call number (sys_exit)
    int     0x80                  ;call kernel

section      .data
msg         db 'Hello, world!',0xa ;our dear string
len         equ $ - msg           ;length of our dear string
```

Security CPU Instructions



AES-NI

- Perform specific AES operation in HW
 - Encrypt/Decrypt round
 - Generate round key

Instruction	Description ^[2]
AESENC	Perform one round of an AES encryption flow
AESENCLAST	Perform the last round of an AES encryption flow
AESDEC	Perform one round of an AES decryption flow
AESDECLAST	Perform the last round of an AES decryption flow
AESKEYGENASSIST	Assist in AES round key generation
AESIMC	Assist in AES Inverse Mix Columns
PCLMULQDQ	Carryless multiply (CLMUL) ^[3]

Security CPU Instructions



AES-NI

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PCLMULQDQ	Carryless multiply (CLMUL) ^[3]

RDRAND

- Read random value from HW and store in given register

RDRAND—Read Random Number

Opcode*/ Instruction
NF _x 0F C7 /6 RDRAND r16
NF _x 0F C7 /6 RDRAND r32
NF _x REX.W + 0F C7 /6 RDRAND r64

RDRAND Leakage



Special Register Buffer Data Sampling (SRBDS) Hardware Vulnerability in Intel CPUs (CVE-2020-0543, aka Crosstalk)

It was **discovered** that special register buffer data of certain Intel CPUs may be exposed to a malicious process executing on the same CPU. Particular processor operations (e.g RDRAND, RDSEED) use data from outside the physical processor core - this can be done via an internal microarchitectural operation called a special register read. This uses part of a shared staging buffer which may not be completely zero'd on subsequent uses by other threads. As such, a local attacker may be able to infer stale values which were previously returned from special register reads to other processors (as their contents may still be present in other parts of the shared staging buffer). Some special register reads return sensitive information (such as RDRAND, RDSEED and SGX EGETKEY) and so an attacker executing code on the same CPU may be able to infer these values for another thread / process executing on the same CPU.

This attack relies on the same techniques used to exploit previous microarchitectural speculative execution vulnerabilities such as **MDS** and **TSX Asynchronous Abort**, and affects some client and Intel® Xeon® E3 processors; it does not affect other Intel Xeon or Intel Atom® processors.

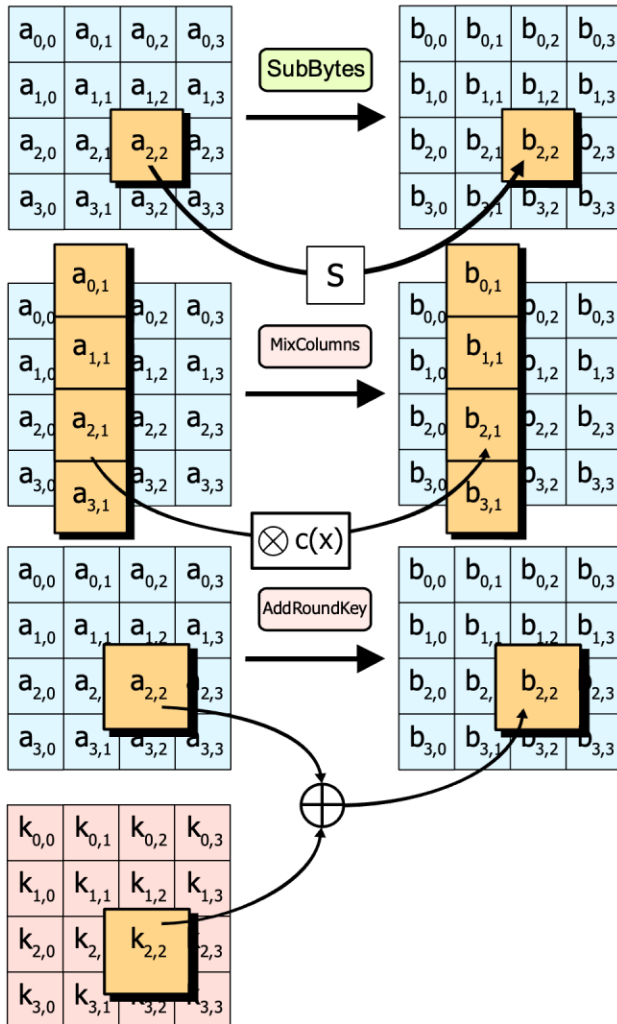
Mitigations for this issue are provided by CPU microcode updates via the `intel-microcode` package. This mitigation consists of ensuring data in the shared staging buffer is overwritten by the RDRAND, RDSEED and EGETKEY instructions and serialising execution of RDRAND etc instructions across multiple logical processors. As a result, this will have an effect on the performance of these instructions. In conjunction, the microcode updates also supports an opt-out mechanism so that performance can be restored if desired - to support this, the Linux kernel supports a kernel command-line option `srbds=off` to allow system administrators to make use of the opt-out mechanism. For details on the boot command line option and how to check system status, please see the [Linux Kernel Special Register Buffer Data Sampling Admin Guide](#).

Oversimplified Descriptions



- **Security CPU Instructions**
 - Trusted actions in standard hardware

Cryptographic Accelerator

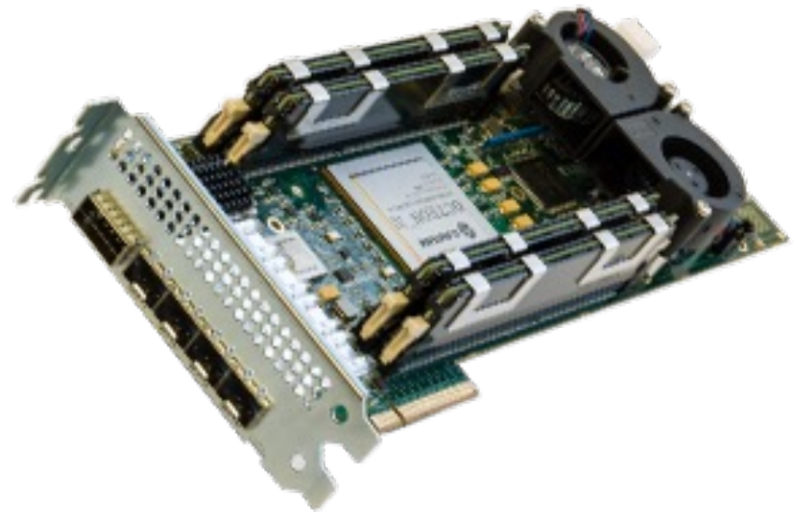


- Operations are often well-defined and repetitive
 - 14-rounds for AES256
 - Trial-and-error for bitcoin mining
 - Standardized protocols
- ASIC allows optimized pipelines for specific behavior

Cryptographic Accelerator



A **Cryptographic Accelerator** is an add-on component that allows software to leverage custom ASICs for improved performance.



Usage: Crypto Accelerator



Primitive-Level Variant

- Offload actions
- Software provides:
 - Action-specific input
 - CT/PT/data/sig+data
 - Instance-specific secret
- Accelerator provides
 - Primitive algorithms
 - Action-specific output

Protocol-Level Variant

- Offload layers
- Software provides:
 - Configuration
 - Long-term secrets
- Accelerator provides:
 - Protocols negotiation
 - Primitive algorithms
 - Short-term secrets
 - Plaintext messages

Oversimplified Descriptions

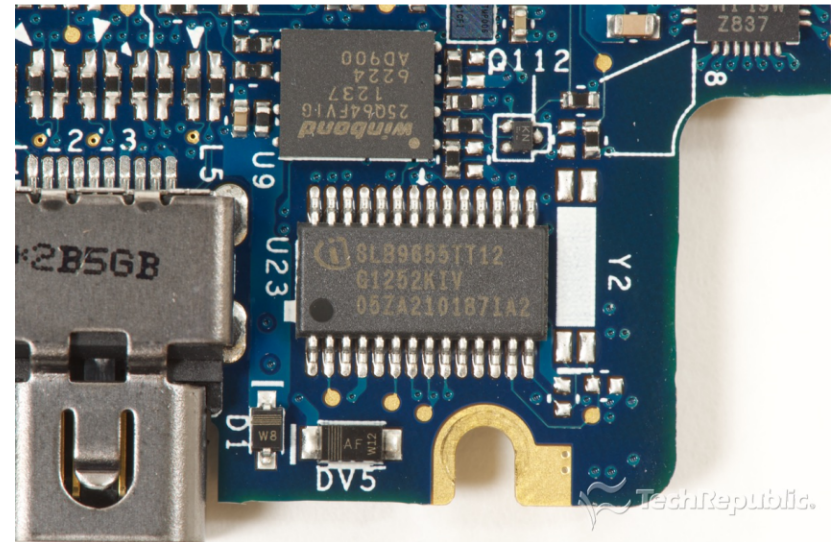


- **Security CPU Instructions**
 - Trusted actions in standard hardware
- **Crypto Accelerator**
 - Fast, trusted actions in add-on hardware

Trusted Platform Module



A **Trusted Platform Module (TPM)** is an additional built-in, self-contained ASIC that provides a central “root of trust” for a device.



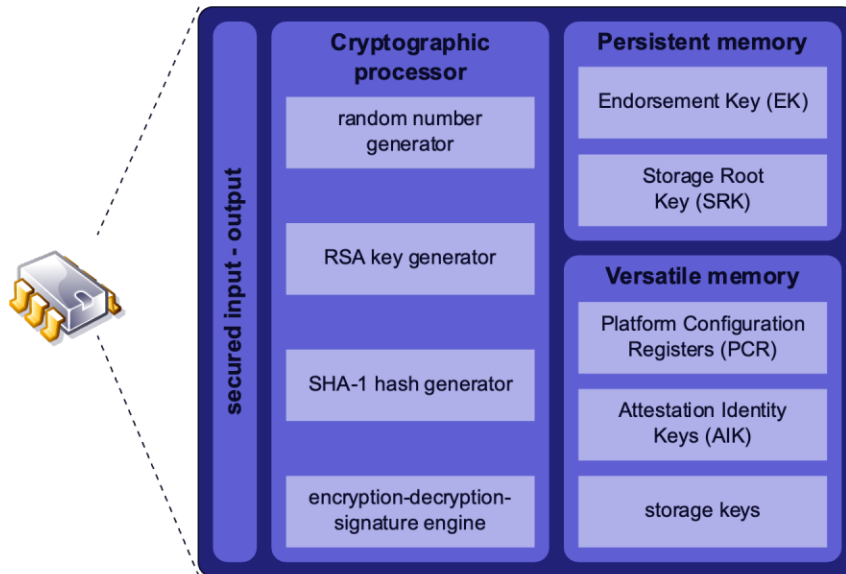
Trusted Platform Module



A Trusted Platform Module (TPM) is additional built-in, self-contained ASIC that provides a central “root of trust” for a device.

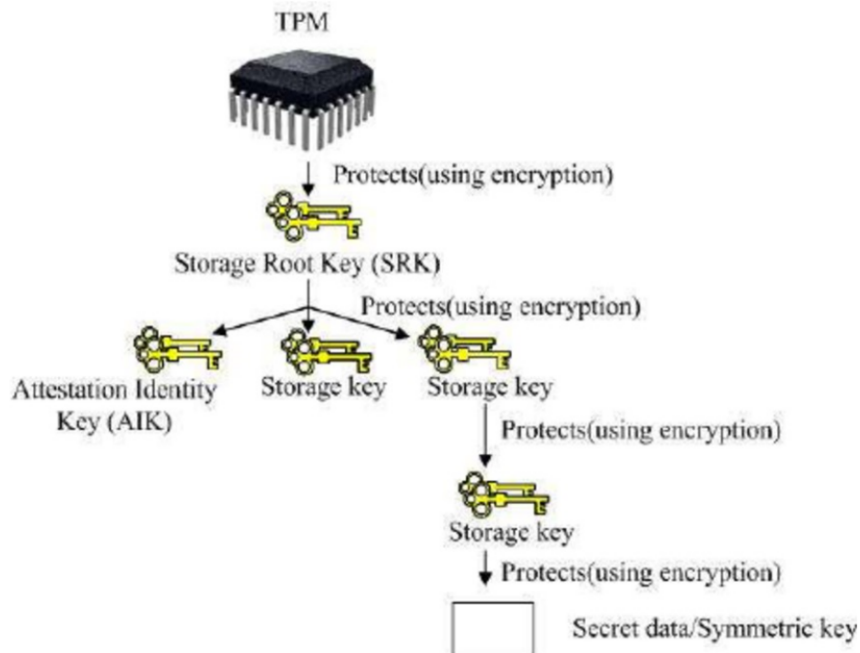


TPM Internals



- Includes suite of crypto primitives
 - RNG
 - Algorithm implementations
 - Secure storage
- Arbitrary control logic
 - Timers, persistent counters, etc

TPM Keys

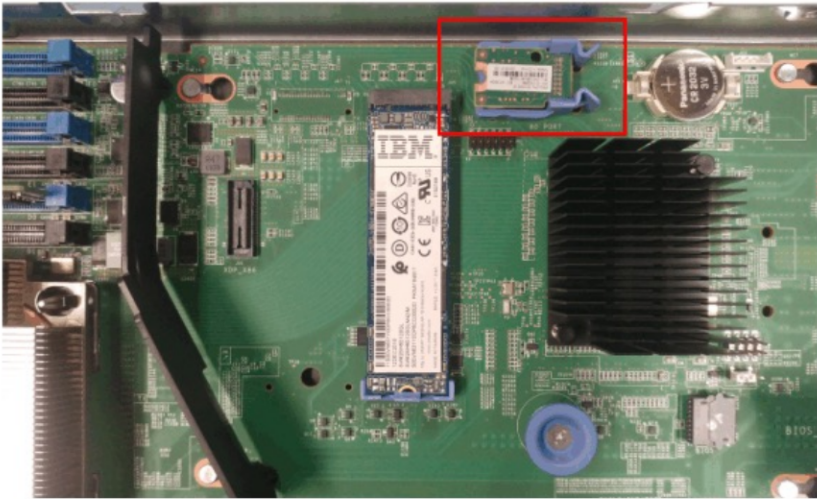


- Secrets are either generated on-board or injected
- Derive many secrets from single root secret via KDF

Usage: Building Block



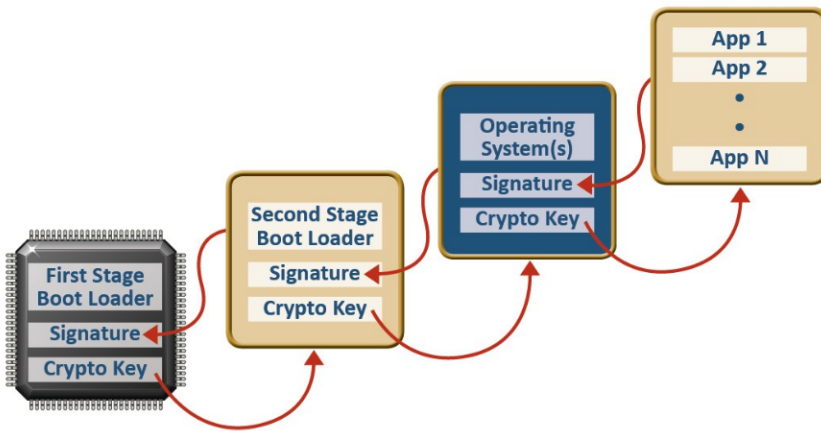
- Most commonly a component on motherboard
- Software treats as black-box operations
 - Hardened, well-defined interface for use



Example: Secure Boot



- TPM validates firmware signature before booting
- If invalid, refuse to launch bootloader
- Used as foundational trust for validating higher-level software



Oversimplified Descriptions



- **Security CPU Instructions**
 - Trusted actions in standard hardware
- **Crypto Accelerator**
 - Fast, trusted actions in add-on hardware
- **Trusted Platform Module**
 - Trusted actions in built-in hardware w/ keys

Hardware Security Module



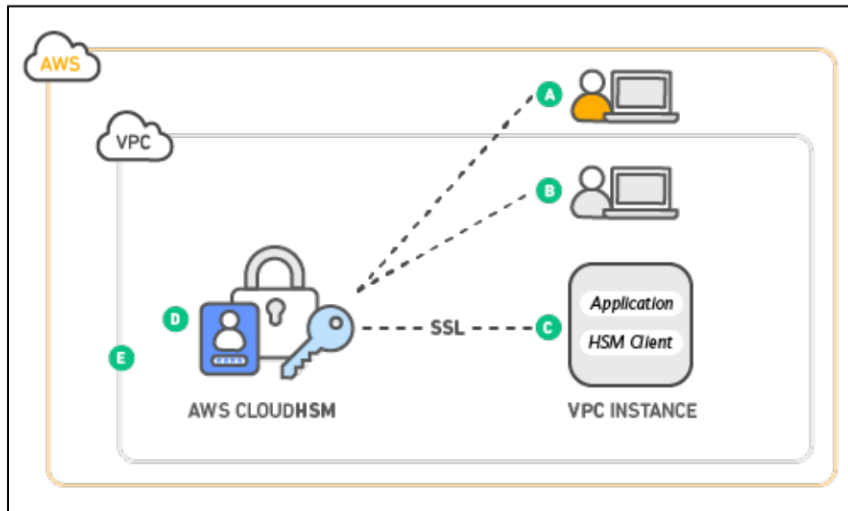
A Hardware Security Module (HSM) is a special-purpose add-on component that securely stores cryptographic keys and performs cryptographic operations.



Hardware Security Module



- High-performance operations
- Restricted logic
 - Most commonly used for signing operations
- Commonly available “in the cloud” for use with AWS/GCP/...



Oversimplified Descriptions

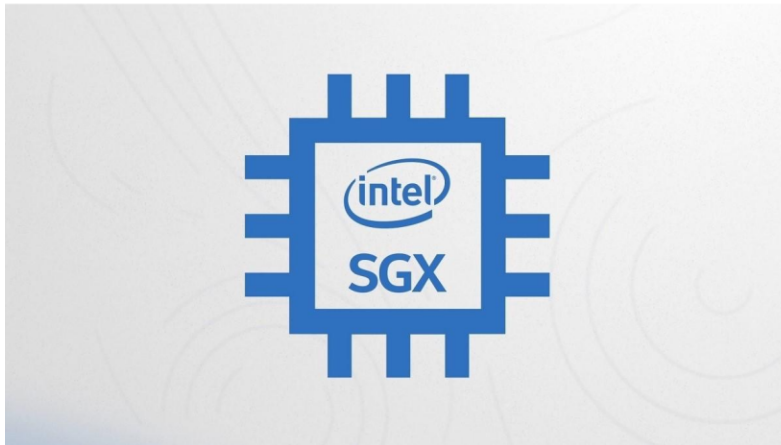


- **Security CPU Instructions**
 - Trusted actions in standard hardware
- **Crypto Accelerator**
 - Fast, trusted actions in add-on hardware
- **Trusted Platform Module**
 - Trusted actions in built-in hardware w/ keys
- **Hardware Security Module**
 - Fast, trusted actions in add-on hardware w/ keys

Trusted Execution Environment



A Trusted Execution Environment (TEE) is a general computation environment that provides additional security properties such as access to keys, memory encryption, etc.



Enclave Logic



```
/*
 * Return a SHA256 hash of the requested key. KEYS SHOULD NEVER BE
 * SENT OUTSIDE THE ENCLAVE IN PLAIN TEXT. This function let's us
 * get proof of possession of the key without exposing it to untrusted
 * memory.
 */
sgx_status_t enclave_ra_get_key_hash(sgx_status_t *get_keys_ret,
    sgx_ra_context_t ctx, sgx_ra_key_type_t type, sgx_sha256_hash_t *hash)
{
    sgx_status_t sha_ret;
    sgx_ra_key_128_t k;

    // First get the requested key which is one of:
    // * SGX_RA_KEY_MK
    // * SGX_RA_KEY_SK
    // per sgx_ra_get_keys().

    *get_keys_ret= sgx_ra_get_keys(ctx, type, &k);
    if ( *get_keys_ret != SGX_SUCCESS ) return *get_keys_ret;

    /* Now generate a SHA hash */

    sha_ret= sgx_sha256_msg((const uint8_t *) &k, sizeof(k),
        (sgx_sha256_hash_t *) hash); // Sigh.

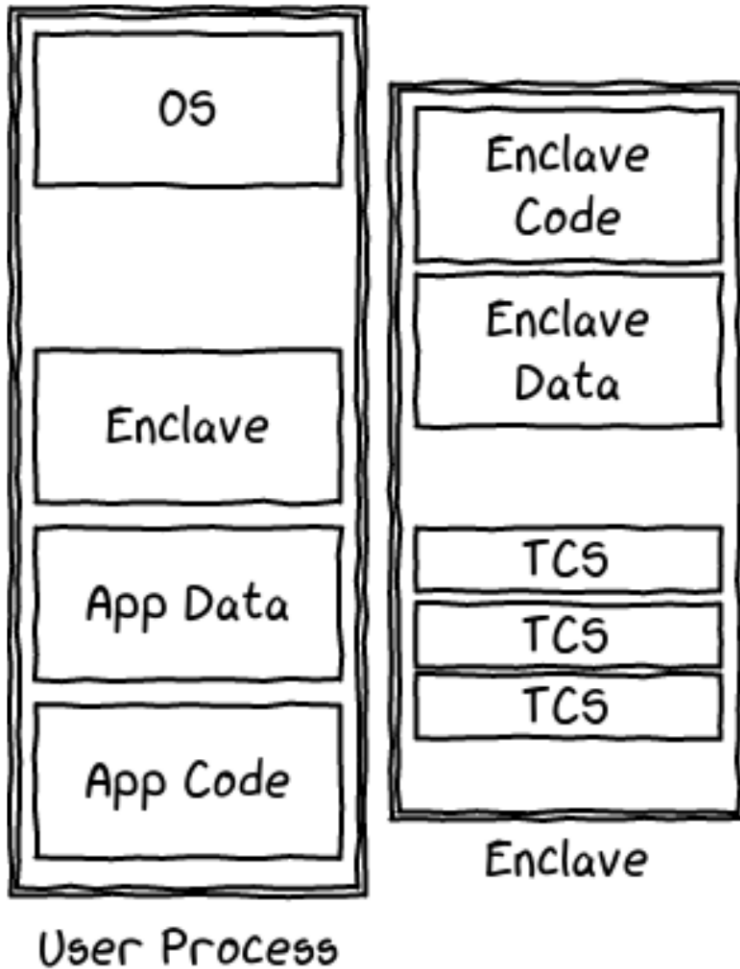
    /* Let's be thorough */

    memset(k, 0, sizeof(k));

    return sha_ret;
}
```

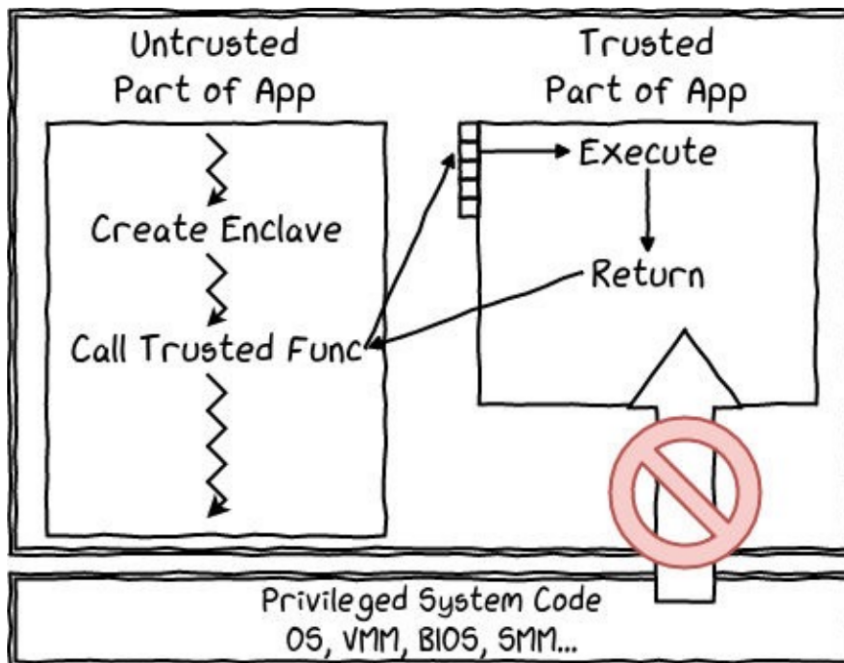
- Allow arbitrary logic from developers
- Extremely small TEE standard library
- Statically compile against TEE standard library & dependencies

TEE Application



- Enclave logic is compiled and signed with enclave key
- Enclave blob compiled into application binary
- Application binary behaves as normal

TEE Operation



- App loads enclave blob via OS driver
- App can make function calls into the enclave
- Enclave executes outside the influence of OS, apps, etc

TEEs in the Real-World



ars TECHNICA SUBSCRIBE SEARCH SIGN IN

RAIDING FORT KNOX —
SGX, Intel's supposedly impregnable data fortress, has been breached yet again

ÆPIC Leak spills users' most sensitive secrets in seconds from SGX enclaves.

DAN GOODIN - 8/9/2022, 12:01 PM



Enlarge

The screenshot shows an article from ars TECHNICA. The header includes the site name, a subscribe button, a search icon, and a sign-in button. The article title is "SGX, Intel's supposedly impregnable data fortress, has been breached yet again" with a sub-headline "ÆPIC Leak spills users' most sensitive secrets in seconds from SGX enclaves." The author is Dan Goodin, dated 8/9/2022. The main image is a stylized blue Intel SGX logo on a light gray background.

BLEEPINGCOMPUTER ☰

Home > News > Security > New Intel chips won't play Blu-ray disks due to SGX deprecation



New Intel chips won't play Blu-ray disks due to SGX deprecation

By **Bill Toulas**

📅 January 14, 2022 ⌚ 11:46 AM 💬 12

The screenshot shows an article from BleepingComputer. The header includes the site name and a menu icon. The breadcrumb trail is "Home > News > Security > New Intel chips won't play Blu-ray disks due to SGX deprecation". There is a printer icon. The article title is "New Intel chips won't play Blu-ray disks due to SGX deprecation" by Bill Toulas. The date is January 14, 2022, at 11:46 AM, with 12 comments. The main image shows two Intel chips on a blue background with binary code.

Oversimplified Descriptions



- **Security CPU Instructions**
 - Trusted actions in standard hardware
- **Crypto Accelerator**
 - Fast, trusted actions in add-on hardware
- **Trusted Platform Module**
 - Trusted actions in built-in hardware w/ keys
- **Hardware Security Module**
 - Fast, trusted actions in add-on hardware w/ keys
- **Trusted Execution Environment**
 - Fast(ish), trusted logic in common hardware w/ keys

Trusted Computing Base



The **Trusted Computing Base (TCB)** is the collection of all components within a system critical to providing security properties.

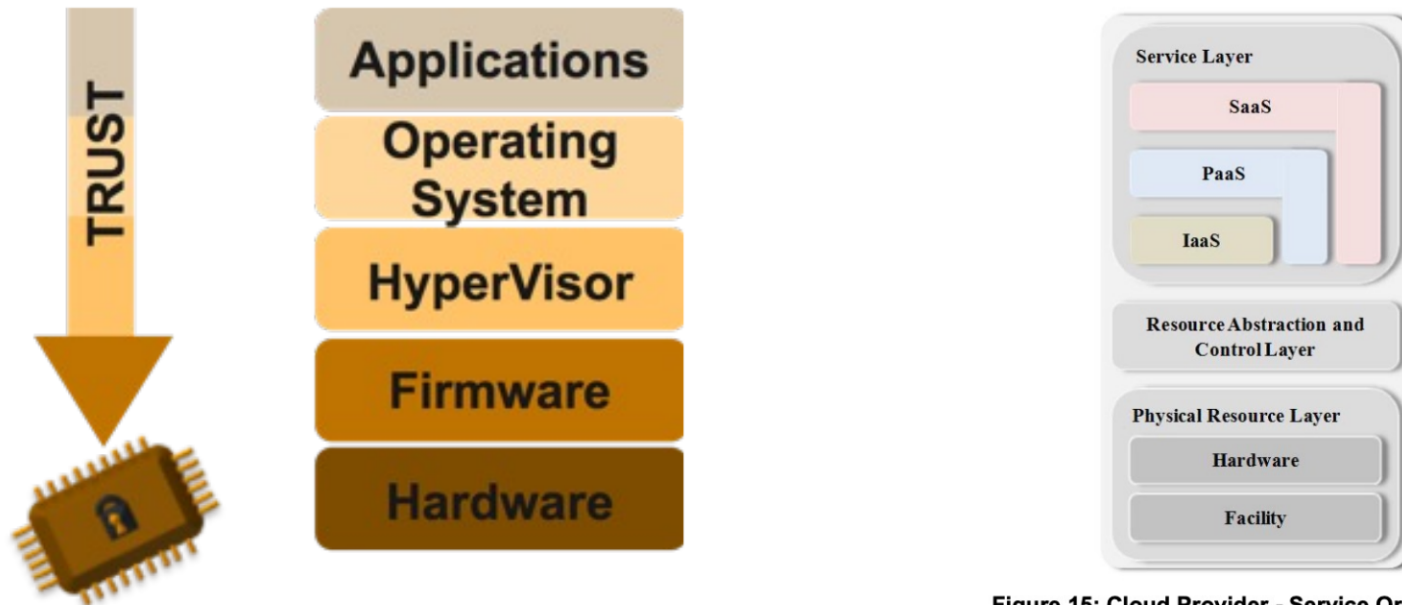
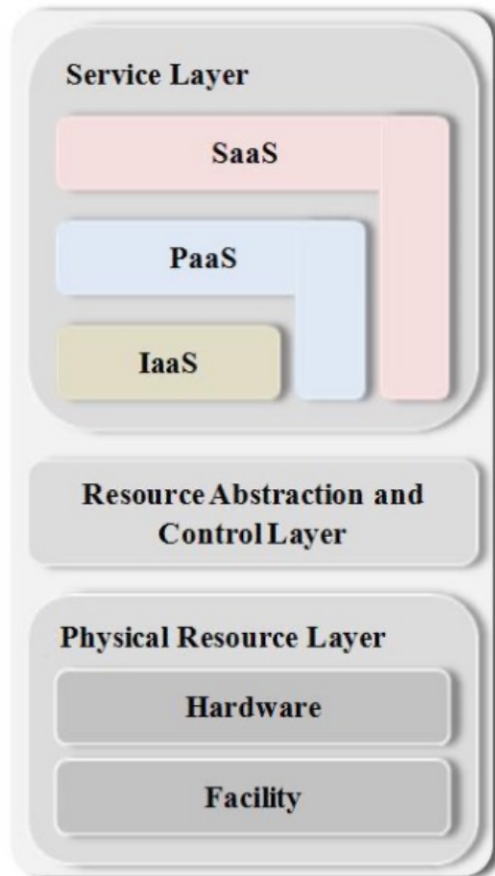


Figure 15: Cloud Provider - Service Orchestration

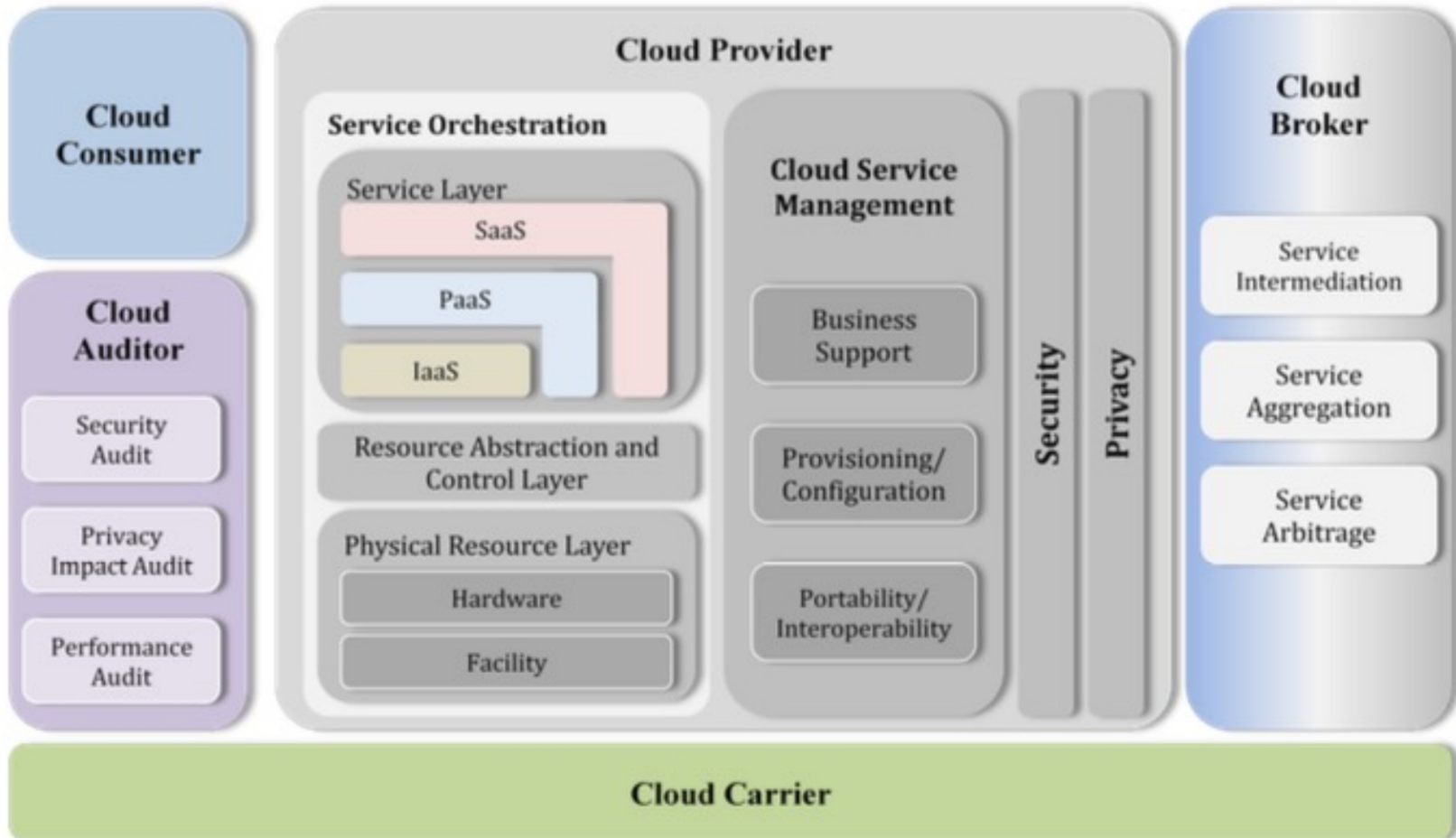
Cloud Provider TCB



- SaaS: Software
 - Office 365
- PaaS: Platform
 - Elastic Container Service
- IaaS: Infrastructure
 - EC2 Instances
- <many more layers of internal services>
- **All on top of Local TCB**

Cloud Computing Architecture

TCB



Computer and Network Security

Lecture 15: Hardware Security/Attacks

COMP-5370/6370
Fall 2024



Evil Maid Attacks



An **Evil Maid Attack** is where an attacker gains temporary physical access to the target's device to exploit or prepare for exploitation.

- Image storage for future forensics
- Completely replace and proxy interaction
- Install firmware-level malware
- Install malicious HW components